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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application of

Applicant : David L. Chapek
Serial No. : 09/605,293
Filed : June 28, 2000
Title : SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY
Docket : MIO 0037 VA
Examiner : N. Drew Richards
Art Unit : 2811

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on June 17, 2002.

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Assistant Commissioner for Patents
Washington, DC 20231

Sir:

BRIEF ON APPEAL

This is an appeal from the Office Action mailed on February 7, 2002, finally rejecting claims 9-12 and 14. A Request for Reconsideration was timely filed on February 21, 2002. An Advisory Action stating that the Request for Reconsideration was not persuasive was mailed on March 15, 2002. A Notice of Appeal was timely filed on April 5, 2002. Our check in the amount of $320.00 accompanies this Brief. 37 CFR §1.17(c).

Real Party In Interest

The real party in interest is the assignee of this patent application, Micron Technology, Inc., by assignment from the named inventor, which assignment has been recorded.

Related Appeals and Interferences

Applicant knows of no related appeals or interferences which would affect the outcome of the present appeal.

Status of Claims

Claims 9-12 and 14 are present in this patent application. Claims 9-12 and 14 stand finally rejected. Accordingly, claims 9-12 and 14 are before this Board on appeal. A correct copy of the appealed claims appears as an Appendix to this Brief.

Status of Amendments

No amendments to the claims after final rejection were filed. All previous amendments have been entered.

Issues Presented

The issues presented for review on appeal are:

(1) Did the Examiner err in rejecting claim 9 as unpatentable under 35 USC §103(a) over "Applicant's admitted prior art"?

(2) Did the Examiner err in rejecting claims 10-12 under 35 USC §103(a) as being unpatentable over Burns et al. in view of "Applicant's admitted prior art"?

(3) Did the Examiner err in rejecting claim 14 under 35 USC §103(a) as being unpatentable over Murata et al. in view of "Applicant's admitted prior art"?

To arrive at a conclusion on issues (1)-(3), the Board must also address the following issue:

(4) Has the Examiner carried his burden of establishing a prima facie case by showing that the teachings of the references are properly combinable and that there existed in the prior art proper motivation and an expectation of success?

Grouping of Claims

The Examiner has rejected claim 9, claims 10-12, and claim 14 on different grounds. Claim 9 has been rejected under 35 USC § 103(a) as being unpatentable over "Applicant's admitted prior art." Claims 10-12 have been rejected under 35 USC §103(a) as being unpatentable over Burns et al. in view of "Applicant's admitted prior art." Claim 14 under 35 USC §103(a) as being unpatentable over Murata et al. in view of "Applicant's admitted prior art." Applicant will argue the patentability of claim 9

separately. Applicant will argue the patentability of claim 10 as representative of claims 10-12. Applicant will argue the patentability of claim 14 separately.

The References

Background of the Invention:

Applicant discusses some current technology in the Background section of the application at page 1, line 12 – page 2, line 21, which the Examiner refers to as "Applicant's admitted prior art." The Background section identifies that Kaufman ion sources are used to pretreat silicon dioxide films with hydrogen ions in order to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon. The hydrogen ion beam pretreatment is typically performed using a Kaufman ion beam source directed normal to the substrate.

Applicant has observed that Kaufman ion sources employ metal grids to accelerate ions at a particular target. During an ion implantation process using a Kaufman ion source, metal from the metal grid sputters off of the grid and becomes implanted in the silicon dioxide, contaminating the surface of the film.

The Background section of the application also discusses Plasma Source Ion Implantation (PSII) stating that PSII has been used to dope various materials, such as tools, aluminum cans and artificial joints, to improve their wear, friction and corrosion properties. PSII is a process by which ions are implanted into a target at energies high enough to bury the ions below the target's surface. To implant the ions in the target, an ionized plasma is formed about the target in an enclosed chamber. A high voltage pulse is applied to the target relative to the conductive walls of the chamber. Ions from the plasma are then driven into the surfaces of the target from all sides simultaneously without any manipulation of the target.

The Background section of the application then discusses two prior patents that use PSII, U.S. Patent Nos. 4,764,394 to Conrad and 5,354,381 to Sheng. Conrad teaches

that PSII may be performed on complex three-dimensional objects formed from materials such as pure metals, alloys, semi-conductors, ceramics and organic polymers. Conrad also teaches that the PSII process taught in the reference provides significant increases in surface hardness of metals and ceramics and provides changes in the optical properties and electrical conductivity of organic polymers. Sheng teaches a PSII apparatus that uses a pair of power supplies and very short ionization negative pulses applied to the cathode underlying the target in conjunction with or followed by short ionization pulses applied to a second cathode which is facing toward the primary (target) electrode to provide neutralizing electrons.

Burns et al.

Burns et al. teaches a field effect transistor having a substrate with a layer of silicon dioxide over the substrate. A thin layer of aluminum is deposited on top of the silicon dioxide layer. See page 177. Burns et al. teaches a read-only memory array wherein the field effect transistor is used. In the positions where a field effect transistor is desired, a thin oxide layer is formed and polysilicon rows act as an effective gate over the region used for the field effect transistor. See page 381.

Murata et al.

Murata et al. teaches a method of fabricating a thin-film transistor which includes the step of forming a source region and a drain region in a semiconductor thin film having a capping film thereon. Murata teaches at figure 6E a microcrystalline silicon film 502 that includes source and drain regions 507a and 507b that are doped with impurity ions. Also shown is an undoped channel region 507 that is formed on a substrate 501. An insulating film 503 is formed to cover the microcrystalline silicon film 502. An interlevel insulating film 508 is formed to cover the gate electrode 504.

Summary of the Invention

Applicant's invention is directed toward semiconductor devices that include a layer of polycrystalline silicon having a smooth morphology. See page specification pages 2-3. Referring to Fig. 1, semiconductor device precursor 10 is provided and

comprises a semiconductor substrate 12, a layer 14 of silicon dioxide 16 formed on the semiconductor substrate 12, the layer 14 of silicon dioxide 16 having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein the layer 14 of silicon dioxide 16 is free of metal contaminants, and a layer 18 of polycrystalline silicon 20 formed on the layer 14 of silicon dioxide 16, the layer 18 of polycrystalline silicon 20 having a smooth morphology. See specification pages 7-10.

Referring to Figs. 2, and 2A – 2C, a field effect transistor 50 having a semiconductor substrate 52 is shown. The surface of the substrate 52 has been implanted with hydrogen ions by PSII and is free of metal contaminants so that the layer 64 of polycrystalline silicon 66 subsequently formed on substrate 52 has a smooth morphology. See specification pages 10-12. A gate oxide 54, a source 56 and a drain 58 are formed in the substrate 52 to form the field effect transistor 50. Referring to Figs. 3A and 4, the field effect transistor 50 described above may be used in a memory array 100. See specification page 12.

Referring to Fig. 5, a thin film transistor 200 is shown including an insulating substrate 202. See specification pages 13-14. A layer 204 of semiconducting material 206 is formed on the surface of the substrate 202. See specification pages 13-14. A source region 208 and a drain region 210 are formed on the layer 204 of semiconducting material 206. See specification pages 13-14. A layer 212 of dielectric material 214 is formed on the layer 204 of semiconducting material 206 and covers the source 208 and the drain 210. See specification pages 13-14. A layer 216 of conducting material 218 is formed on the layer 212 of dielectric material 214 to form a gate electrode 220. See specification pages 13-14. The insulating substrate 202 has been doped with hydrogen ions. See specification pages 13-14.

Summary of the Argument

The Examiner has not carried his burden of establishing the necessary prima facie case of obviousness. No motivation or suggestion exists to combine the prior art in the manner asserted by the Examiner. No motivation or suggestion exists to combine the

prior art with Burns et al. No motivation or suggestion exists to combine the prior art with Murata et al.

ARGUMENT

I. Establishing a *prima facie* case of obviousness.

In order to establish a prima facie case of obviousness, the Examiner has the burden of proving, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the reference itself or in the knowledge available in the art, to modify that reference's teachings; 2) there is a reasonable expectation on the part of the skilled practitioner that the modification or combination has a reasonable expectation of success; and 3) the prior art reference must teach or suggest all of the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Both the teaching or suggestion and the reasonable expectation of success must be found in the prior art and not based on an applicant's disclosure. *Id.*

In carrying this burden, the Examiner "must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious." Ex parte Clapp, 227 USPQ 972, 973 (PTOBPAI 1985). A rejection based on § 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. *In re Warner*, 154 USPQ 173, 178 (CCPA 1967). The Examiner may not, because he may doubt that the invention is patentable, resort to speculation, unfounded assumptions, or hindsight reconstruction to supply deficiencies in his required factual basis. *Id.*

II. The prior art discussed in the Background section of the specification is not properly combinable to reject claim 9.

The Examiner rejected claim 9 asserting that it would have been obvious to use PSII to implant hydrogen ions in a layer of silicon dioxide on a semiconductor substrate, the motivation being to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities. Applicant submits that no *prima facie* case of obviousness has been established for the present claims over the prior art of

record. The present invention teaches a semiconductor precursor device where the silicon oxide surface is implanted with hydrogen ions from PSII to provide a smooth surface morphology for a subsequently deposited polysilicon layer by decreasing surface contamination. The prior art does not teach or suggest the claimed invention.

Applicant discusses some current technology in the Background section of the application at page 1, line 12 – page 2, line 21, which the Examiner refers to as "Applicant's admitted prior art." There is a key dispute between the Examiner and applicant over what has been "admitted" to be in the prior art. Applicant admits that Kaufman ion sources were used to implant hydrogen ions into silicon dioxide films. Applicant also admits that PSII exists as a technique used to dope various materials such as tools, aluminum cans, and artificial joints. Applicant does not admit that the prior art of record recognized the problem of metal contamination when using a Kaufman ion source. Also, applicant does not admit that the prior art of record used PSII as a technique in fabricating semiconductor devices such as FETs and memories.

Furthermore, the Examiner makes at least two incorrect assertions in the final rejection. First, the Examiner asserts in the final rejection that the "admitted prior art" at page 1, lines 12-16, teaches a polycrystalline silicon having a smooth morphology. However, the Background section at page 1, lines 12-16 teaches pretreating silicon dioxide films with hydrogen ions to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Second, the Examiner asserts in the final rejection that the "admitted prior art" teaches the use of PSII to implant which results in the silicon dioxide layer being free of metal contaminants. The Background section states that PSII is a process by which ions are implanted into a target at energies high enough to bury the ions below the target's surface and that PSII exists as a technique used to dope various materials such as tools, aluminum cans, and artificial joints. However, the Background section does not explicitly teach the use of PSII to treat a silicon dioxide layer, nor does it state that PSII results in a silicon dioxide layer being free of metal contaminants.

The Examiner is not permitted to use the Background section of the application as a basis for finding teaching or suggestion. As stated above, both the teaching or suggestion and the reasonable expectation of success must be found in the prior art and not based on an applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Background section of the application is provided to describe the extent practical the state of the prior art. See MPEP §608.01(c). The Background section may also point out "the problems involved in the prior art or other information disclosed which are solved by the applicant's invention." See MPEP §608.01(c).

Even if the Examiner does use the "admitted prior art" in the Background section of the application, no motivation or suggestion is found. The Examiner asserts two different bases for motivation or suggestion, one in the final rejection and one in the Advisory Action. In the final rejection, the Examiner asserts that the motivation or suggestion to combine the "admitted prior art" is to provide a layer with increased surface hardness and improved optical properties, taken from page 2, lines 12-14 of the Background section. See Final Rejection, page 3. Providing a layer with increased surface hardness and improved optical properties cannot be proper motivation or suggestion to combine the "admitted prior art" because the claimed invention does not require these properties. Rather, claim 9 recites a semiconductor with a layer of polycrystalline silicon having a smooth morphology. There is no motivation to improve surface hardness and no motivation to improve optical properties because these are not properties that are needed by the semiconductor device as claimed.

The Examiner's argument fails because the "admitted prior art" lacks the suggestion and motivation to combine their teachings to obtain the same result as the claimed invention. The Examiner states in his Advisory Action that motivation is provided because the "admitted prior art" recognized the shortcoming of metal contamination, therefore, one skilled in the art would be motivated to rectify the shortcoming. Applicant has recognized the problem that metal contamination exists if a Kaufman ion source is used to implant silicon dioxide films with hydrogen ions in the Background section. Applicant then explains that PSII is used to dope various materials

such as tools, aluminum cans, and artificial joint to provide a layer with increased surface hardness and improved optical properties. The Examiner has improperly used applicant's own disclosure and recognition of the problem solved by the claimed invention. Thus, the necessary motivation or suggest does not exist in the prior art.

Even if motivation or suggestion to rectify this shortcoming did exist, there is no motivation to rectify the metal contamination problem by implanting hydrogen ions using PSII. The Background section of the application teaches the use of a Kaufman source with hydrogen ions in order to pretreat silicon dioxide films and prepare the surface of a silicon dioxide film for the deposition of a layer of polycrystalline silicon. The pretreatment provides for a thinner and smoother polycrystalline silicon film. Then the Background section states that hydrogen ions may be implanted by PSII into a target in order to obtain a hard surface or to provide neutralizing electrons. However, there is no teaching, nor any indication of a desire to teach implanting hydrogen ions into a silicon dioxide film by PSII to obtain a subsequently deposited polysilicon layer with a smooth surface that is free of metal contamination.

Applicant submits that it would not have been obvious to one of ordinary skill in the art to use PSII to implant the hydrogen ions because the prior art does not teach or suggest using the same methods to obtain the same desired result as the claimed invention. The present invention teaches implanting plasma hydrogen ions uniformly on a silicon dioxide surface to provide a smooth surface morphology for a subsequently deposited polysilicon layer by decreasing surface contamination, specifically metal contamination. The "admitted prior art" does not teach or suggest the claimed invention.

III. The "admitted prior art" does not suggest the desirability of combining the "admitted prior art" teachings nor does the "admitted prior art" present a reasonable expectation of success.

The Examiner has attempted to combine two unrelated teachings in an effort to arrive at the claimed invention. The mere fact that the references can be combined does

not render the resultant combination obvious unless that prior art also suggests the desirability of the combination. In re Mills, 16 USPQ2d 1430 (Fed. Cir. 1990) and MPEP §2143.01. The desirability of the combination is not suggested in the prior art, therefore, the Examiner's proposed combination is based on prohibited hindsight.

In the Advisory Action, the Examiner states that the Kaufman ion source implantation is related to PSII because they are both well known methods for implanting ions into a substrate. Although the Kaufman ion source and PSII are both used to implant ions into a substrate, they are still two very different methods. The Kaufman ion source uses a metal grid to bombard the substrate with a hydrogen ion beam. PSII implants ions into a substrate by forming an ionized plasma around the substrate in an enclosed chamber. A high voltage pulse is applied to the substrate which drives the ions from the plasma into the surfaces of the substrate simultaneously with out manipulating the substrate. Clearly, the Kaufman method and PSII use two completely different approaches to implant ions into a target.

Courts have found patentable subject matter where the invention is "close on the surface" to the prior art, "but where the small difference has eluded those of ordinary skill in the art in search of the solution to a persistent problem." In re Palmer, 451 F.2d 110, 1102-03, 172 USPQ 126, 128 (Fed. Cir. 1971); citing United States v. Adams, 383 U.S. 39, 148 USPQ 479 (1966), Eibel Process Co. v. Minnesota & Ontario Paper Co., 261 U.S. 45 (1923).

The present invention addresses the need for a smooth morphology with reduced surface contamination, namely metal contamination. The Examiner states that this problem is recognized on page 1, lines 18-23 of the prior art and would have been obvious to one of ordinary skill in the art to solve the problem. As stated above, the Background section may point out "the problems involved in the prior art other information disclosed are solved by the applicant's invention should be indicated." See MPEP §608.01(c). Applicant identified the problem of metal contamination occurring when the Kaufman ion source is used to implant hydrogen ions in a substrate. The

Examiner has improperly used applicant's disclosure and identification as a basis for finding motivation. Furthermore, the Background section does not teach or suggest using PSII to correct this deficiency, thus it would not have been obvious to use PSII to implant the hydrogen ions in order to avoid metal contamination and provide a smooth surface. Rather the Background section only teaches using PSII to improve surface harness and optical properties. Thus, there is no motivation to combine the "admitted prior art."

There is also no reasonable expectation of success. The Kaufman ion source implants hydrogen ions into a layer of silicon dioxide to provide a for a thinner and smooth polycrystalline silicon film. There is no indication that the PSII would be expected by one skilled in the art to provide a successful way of implanting hydrogen ions which would provide a smooth surface morphology for subsequently deposited polysilicon layer in a semiconductor device precursor. The Examiner asserts that there is a reasonable expectation of success because the metal contamination comes from the metal grid, thus using PSII without a metal grid would not cause contamination. The problem of metal contamination and the need for a smooth surface is not addressed in the generalized explanation of PSII in the Background section of the application. Rather PSII is discussed only as providing a hard surface with improved wear and corrosion properties. There is no indication that PSII, when used with hydrogen ions and used to treat a silicon dioxide film, would permit the later deposition of a polysilicon layer with a smooth morphology. Thus, simply because PSII does not use a metal grid to implant ions into a substrate does not provide a reasonable expectation that PSII can be used to provide a smooth surface free of contaminants on a layer of silicon dioxide. Even if it may have been obvious from the Background section of the application to try to implant hydrogen ions by using PSII into a silicon dioxide layer to produce a polysilicon layer with a smooth morphology, obvious to try is not the standard.

While the present invention may take steps from individual prior art teachings, the present invention produces a different invention than that taught by the prior art. Considering that the teachings of the prior art for PSII are not applicable to the teachings of the prior art for the Kaufman ion source, the Examiner has used prohibited hindsight in

order to combine the prior art teachings in the Background section of the application. Because the prior art does not teach or suggest the present invention, and the prior art does not express any desirability or motivation to combine their teachings, nor provide any expectation of success, the Examiner has failed to establish the necessary prima facie case for obviousness.

IV. Burns et al. and the admitted prior art are not properly combinable.

Claims 10-12 have been rejected under 35 USC §103(a) as being unpatentable over Burns et al. in view of applicant's "admitted prior art." The Examiner asserts that Burns et al. teaches a field effect transistor having a substrate with a layer of silicon dioxide over the substrate and that the layer of silicon dioxide is covered by a layer of polycrystalline silicon, pointing to page 381 and Figure 9.8 of Burns et al. The Examiner also admits that Burns et al. does not teach implanting hydrogen ions into the silicon dioxide.

Burns et al. teaches a field effect transistor with a thin oxide layer formed so that polysilicon rows can act as an effective gate over the region. The "admitted prior art" is explained above. Claim 10 recites a field effect transistor that includes "a layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of metal contamination in the layer."

As shown above, there is no motivation or suggestion in the "admitted prior art" to use PSII to implant hydrogen ions in a silicon dioxide film to permit the later deposition of a polysilicon layer with a smooth morphology. Burns et al. does not cure this deficiency. In fact Burns et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination or the use of PSII to implant hydrogen ions. Thus, the "admitted prior art" and Burns et al. cannot properly be combined to render claims 10-12 obvious.

V. Murata et al. and the admitted prior art are not properly combinable.

The Examiner also rejected claim 14 under 35 USC §103(a) as being unpatentable over Murata et al. (US Patent No. 5,576,229) in view of "Applicant's admitted prior art." The Examiner claims that Murata et al. and the prior art are combinable because they are from the same field of endeavor and that at the time of the invention it would have been obvious to a person ordinary skill in the art to implant hydrogen ions into the glass substrate. The Examiner asserts that the motivation for combining the references is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon in order to provide for a thinner and smoother polycrystalline silicon film. The Examiner further states that it would have been obvious to a person of ordinary skill in the art to implant the hydrogen atoms by PSII. The motivation is to provide a layer with increased surface hardness and improved optical properties as well as avoiding metal impurities.

Murata teaches at figure 6E a microcrystalline silicon film 502 that includes source and drain regions 507a and 507b that are doped with impurity ions. Also shown is a channel region 507 not doped with impurity ions that is formed on a substrate 501. An insulating film 503 is formed to cover the microcrystalline silicon film 502. An interlevel insulating film 508 is formed to cover the gate electrode 504. The "admitted prior art" is explained above.

As discussed above, there is no motivation or suggestion in the "admitted prior art" to use PSII to implant hydrogen ions in a silicon dioxide film to permit the later deposition of a polysilicon layer with a smooth morphology. In addition, the Examiner's reasons for motivation, providing a layer with increased surface hardness and improved optical properties, cannot be proper motivation or suggestion to combine the "admitted prior art" because the claimed invention does not require these properties. Rather, claim 14 recites a semiconductor with a layer of polycrystalline silicon having a smooth morphology. There is no motivation to improve surface hardness and no motivation to improve optical properties because these are not properties that are needed by the

semiconductor device as claimed. Murata et al. does not solve the deficiency of the "admitted prior art." In fact Murata et al. does not even teach or suggest anything related to a smooth surface morphology with no metal contamination. Thus, the "admitted prior art" and Murata et al. cannot be properly be combined to render claim 14 obvious.

VI. Conclusion

For all of these reasons, Applicant submits that the rejections are not well taken and all rejections of claims 9-12 and 14 should be reversed in their entirety by this Board.

Respectfully submitted,

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